REMARKS

The Office Action dated October 30, 2003, has been received and carefully noted. The above amendments to the title and specification, and the following remarks, are submitted as a full and complete response thereto. Claims 1-58 are pending in the above-cited application and again submitted for consideration.

The Office Action contained several objections, including objections to the title, the specification and the abstract. Applicants have amended the title, amended the first paragraph of the specification and submit herewith a replacement abstract that corrects a minor error in the original abstract. Reconsideration and withdrawal of the objections are respectfully requested.

The Office Action notes that claims 24-32, 36, 39, 44, 45, 47, 48, 51 and 52 contain allowable subject matter and would be allowed if rewritten in independent form. Applicants wish to thank the Examiner for so indicating and Applicants address the independent claims, from which the allowable claims depend, below.

Certain claims of the present application were rejected in several rejections applying many references. Claims 1-7 and 53 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Larson* (U.S. Patent No. 4,424,565) in view of *Warner et al.* (U.S. Patent No. 6,289,015). Claims 8-16 and 54 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Warner et al.* in view of *O'Donnell et al.* (U.S. Patent No. 6,381,642). Claims 17-22 and 55 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Larson* in view of *O'Donnell et al.* Claims 46, 49, 50 and 58 were

rejected under 35 U.S.C. §103(a) as being unpatentable over *Larson* in view of *O'Donnell et al.* and *Bellanger* (U.S. Patent No. 6,256,306). Claims 23, 33, 34, 35 and 56 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Larson* in view of *Warner et al.* and *Bellanger*. Claims 37, 38, 40-43 and 57 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Warner et al.* in view of *O'Donnell et al.* and *Bellanger*. The above rejections are respectfully traversed based on the remarks that follow.

The instant application claims priority, in part, from United States Provisional Patent Applications: Serial No. 60/141,496, filed on June 28, 1999, and Serial No. 60/155,104, filed on September 22, 1999. The instant application is also a continuation-in-part of United States patent application Serial No. 09/343,409, filed on June 30, 1999, now U.S. Patent 6,177,566. *O'Donnell et al.*, cited above, was filed October 21, 1999 and cannot be applied as prior art against the instant application under 35 U.S.C. §§102 and 103. With respect to the claims rejected over *O'Donnell et al.,* the subject contained in those claims finds support in the above-noted applications which have effective filing dates that are before the effective filing date of *O'Donnell et al.* As such, Applicants respectfully assert that all of the rejections relying on *O'Donnell et al.* are improper and should be withdrawn. Thus, claims 8-22, 37-52, 54, 55, 57 and 58 are not rejected over prior art and should be allowed.

The present invention is directed, according to claim 1, to a method of processing internal operations in a network switch. The method includes the step of constructing a

lookup table in system memory, by snooping a communication channel in a network switch for lookup table information, and, upon detection of lookup table information on the communication channel, transmitting the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory. The method also includes the step of processing DMA operations by providing a DMA descriptor including a reload field therein, processing the DMA descriptor, and identifying a location of a next DMA descriptor based upon a condition of the reload field. The lookup table in remote system memory enables CPU access to the lookup table without requiring communication on the communication channel and the condition of the reload field enables flexible DMA descriptor handling.

The present invention is directed, according to claim 23, to a method of processing packets in a network switch. The method includes the steps of inserting a stack-specific tag into a packet, processing the packet in a stack of network switches in accordance with tag information in the stack-specific tag and removing the stack-specific tag from the packet. The method includes constructing an address lookup table for the network switch in a system memory, the method of constructing the address lookup table comprising the steps of snooping a communication channel in a network switch of the stack of network switches, for address lookup table information being communicated thereupon, and upon detection of address lookup table information on the communication channel, transmitting the address lookup table information to a remote system memory, thereby constructing an address lookup table in the remote system memory. The method also

includes processing DMA operations by providing a DMA descriptor including a reload field therein, processing the DMA descriptor, and identifying a location of a next DMA descriptor based upon a condition of the reload field. The lookup table in remote system memory enables CPU access to the lookup table without requiring communication on the communication channel and the condition of the reload field enables flexible DMA descriptor handling.

The present invention is directed, according to claim 53, to a network switch for handling packets. The network switch includes at least one lookup table therein, the lookup table being constructed based upon lookup messages transmitted over an internal communication channel and snoop logic connected to a remote system memory, the snoop logic also being connected to the internal communication channel to detect lookup table information being transmitted on the channel, and transmit the lookup table information to the remote system memory. The snoop logic creates a duplicate lookup table in the remote system memory for direct memory access by a remote CPU. The network switch also includes a DMA unit containing DMA descriptor information therein, the DMA descriptor information including a reload field and a DMA processing unit for processing the DMA descriptor information, the DMA processing unit identifying a location of a next DMA descriptor based upon a condition of the reload field, the DMA unit and the DMA processing unit enabling efficient access to the remote system memory.

The present invention is directed, according to claim 56, to a network switch. The network switch includes a tag insertion unit for inserting a stack specific tag into a packet, a processing unit for processing the packet in a stack of network switches in accordance with tag information in the stack-specific tag, a removing unit for removing the stack-specific tag from the packet when the packet is being switched to a destination port and at least one lookup table, the lookup table being constructed based upon lookup messages transmitted over an internal communication channel in the network switch. The network switch also includes snoop logic connected to a remote system memory, the snoop logic also being connected to the internal communication channel to detect lookup table information being transmitted on the channel, and transmit the lookup table information to the remote system memory, a DMA unit containing DMA descriptor information therein, the DMA descriptor information including a reload field and a DMA processing unit for processing the DMA descriptor information, the processing unit identifying a location of a next DMA descriptor based upon a condition of the reload field. The DMA unit and the DMA processing unit work in conjunction with the remote system memory and the snoop logic creates a duplicate lookup table in the remote system memory for direct memory access by a remote CPU.

In the rejection of claims 1-7 and 53, the Office Action cites both *Larson* and *Warner et al.* *Larson* is directed to a channel interface circuit that functions in a multiprocessor environment to provide a high speed interface between a processor and a communication channel. The rejection cited Fig. 7 as illustrating the loading of table

contents into a Direct Memory Access (DMA) control table, where the processor need not use the communication channel to communicate with the table. The rejection acknowledges that *Larson* fails to teach or suggest snooping the communication channel for lookup table information and thus also cited *Warner et al.*

Warner et al. is directed to a method and apparatus for secure switching of packets within a communications network. The reference discloses that the switch includes address matching logic that implements an address lookup scheme. *Warner et al.* discloses snooping a bus on which an indication of an active port is provided to determine whether the packet was received at the first port and to determine source and destination addresses for the packet. The Office Action also alleges that *Warner et al.* teaches transmitting the lookup table information to a remote system memory because the address-lookup device (86) is connected to an EEPROM (104). With respect to at least the last allegation, Applicants respectfully assert that the Office Action is mistaken.

Warner et al. discusses the connection between the address-lookup device and the EEPROM at column 5, lines 11-18: "The address-lookup device 86 is also shown to be coupled to an EEPROM 104, that stores a sequence of initialization codes 106 *that allow the address-lookup device 86 to be auto-configured.* In an alternative embodiment of the present invention, initialization data may be downloaded to the address-lookup device 86 from a microprocessor (not shown) coupled to the address-lookup device 86." (Emphasis added). The disclosure of *Warner et al.* does not suggest that any lookup table information is transferred to the EEPROM; rather, the disclosure provides that data from

the EEPROM is transferred to the address-lookup device as part of the latter's initialization.

Claim 1 recites, in part, "transmitting the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory," with a similar limitation found in claim 53. Applicants respectfully assert that *Warner et al.* fails to teach or suggest this element because there is no disclosure of data being transferred from the address-lookup device to the EEPROM. Additionally, there is no disclosure in *Warner et al.* that a lookup table would be reconstructed in the EEPROM, as required by claims 1 and 53. *Larson* also fails to teach or suggest these elements of those claims. As such, Applicants respectfully assert that the rejection of claims 1-7 and 53 is improper for fialing to teach or suggest all of elements of those claims and reconsideration and withdrawal of the rejection are respectfully requested.

With respect to the rejection of claims 23, 33, 34, 35 and 56, the Office Action acknowledges that *Larson* and *Warner et al.* fail to teach or suggest all of the elements of those claims and cites *Bellanger* in the rejection. *Bellanger* is cited for its alleged use of tagging of packets in the handling flows of the packets through a network switch. However, even if *Bellanger* was accepted as teaching what has been alleged, which Applicants do not admit, it would still not teach all of the elements of claims 23 and 56.

The claims recite, in part, inserting a *stack specific* tag into a packet and processing the packet in a *stack of network switches* in accordance with tag information in the stack-specific tag, or elements that perform those processes, in claim 56. There is

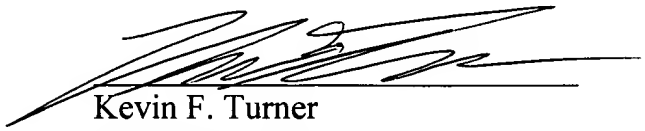
nothing in *Bellanger*, nor *Larson* and *Warner et al.*, that teaches or suggests the use of stacked network switches and the use of stack tags in processing packets in the stack. While *Bellanger* could possibly be used to teach the use of tags in processing the flows of packets, *Bellanger* fails to teach or suggest the elements of 23 and 56 recited therein. For this reason, Applicants respectfully assert that the rejection of claims 23, 33-35 and 56 is improper and reconsideration and withdrawal are respectfully requested.

To conclude, since claims 8-22, 37-52, 54, 55, 57 and 58 are not rejected over prior art, claims 24-32, 36, 39, 44, 45, 47, 48, 51 and 52 were indicated as containing allowable subject matter, and the rejections of 1-7, 23, 33-35, 53 and 56 have been shown to be improper, claims 1-58 should now be allowed. Further, Applicants respectfully request that the application be allowed to proceed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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